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WORKMAN NYDEGGER
60 EAST SOUTH TEMPLE
1000 EAGLE GATE TOWER
SALT LAKE CITY, UT 84111

EXAMINER	
LEUNG, CHRISTINA Y	
ART UNIT	**PAPER NUMBER**
2613	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,250	SASSER ET AL.	
	Examiner	Art Unit	
	Christina Y. Leung	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2-9-07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 6, 13, 21, 38-46, and 50-52** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 6, 21, and 38 each recite "substantial conformity with the SFF configuration standard." **Claims 39-46 and 50-52** depend on claim 38 and therefore also recite this limitation. Similarly, **claim 13** recites "the serial digital interface substantially conforms to one of a GBIC standard; and, the SFF standard." The claims are indefinite because they refer to industry standards. Since the organizations implementing standards may change them, any connection a claim may have to these standards may have varying scope over time. It is inappropriate to have the scope of the claim change over time. Furthermore, if the standard changes, the disclosure may no longer support the limitation and may become non-enabling.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. **Claims 1, 2, 4-6, 8-11, 13-17, 19-21, 23-25, 27, 29, 31-39, 41, 42, 44-47, 49, 50, and 52** are rejected under 35 U.S.C. 102(a) as being anticipated by **SFF Committee** ("SFF-8053 Specification for GBIC (Gigabit Interface Converter) Rev. 5.5," September 27, 2000).

Regarding **claim 1**, SFF Committee discloses an optoelectronic module (page 4, Figure 1), comprising:

a housing (page 21, Figure 11);

an optoelectronic component (including "Optical Receiver" and "Laser" as shown in Figure 1) substantially disposed within the housing;

a controller IC (including "Laser Drive Safety Control" in Figure 1) disposed within the housing and including a serial digital interface configured to facilitate communication, between the optoelectronic module and a host, of diagnostic parameter information concerning the optoelectronic component; and

a pinout arrangement comprising:

a pin array having a plurality of pins ("20-pin SCA-2 Connector to Host" in Figure 1), at least some of which are in communication with the controller IC; and a pair of pins (serial clock signal "SCL" on pin 5 and serial data signal "SDA" on pin 6) in communication with the serial digital interface, each of the pair of pins also being configured and arranged for communication with the host by way of a corresponding interface line (pages 12-13, Table 8 and "5.2.1 Serial module definition protocol" and pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)")

Regarding **claim 17**, SFF Committee discloses an optical transceiver module (page 4, Figure 1), comprising:

a housing (page 21, Figure 11);

a transmit optical subassembly ("Laser" as shown in Figure 1) substantially disposed within the housing;

a receive optical subassembly ("Optical Receiver" as shown in Figure 1) substantially disposed within the housing;

a controller IC (including "Laser Drive Safety Control" in Figure 1) and including a serial digital interface configured and arranged to facilitate communication, between the optical transceiver module and a host, of diagnostic parameter information relating to at least one of: the transmit optical subassembly; and, the receive optical subassembly; and

a plurality of memory mapped locations (in an E^2PROM; pages 12-13, "5.2.1 Serial module definition protocol"; and pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)"), at least one of which is configured to store diagnostic parameter information and is accessible by way of the serial digital interface; and

a pinout arrangement comprising:

a pin array having a plurality of pins ("20-pin SCA-2 Connector to Host" in Figure 1), at least some of which are in communication with the controller IC, and

a pair of pins in communication with the serial digital interface (serial clock signal "SCL" on pin 5 and serial data signal "SDA" on pin 6), each of the pair of pins also being configured and arranged for communication with the host by way of a corresponding interface line (pages 12-13, Table 8 and "5.2.1 Serial module definition protocol").

Regarding **claim 38**, SFF Committee discloses an optoelectronic module (page 4, Figure 1), comprising:

a housing (page 21, Figure 11);

an optoelectronic component (including "Optical Receiver" and "Laser" as shown in Figure 1) substantially disposed within the housing;

a controller IC (including "Laser Drive Safety Control" in Figure 1) disposed within the housing and including a serial digital interface configured to facilitate communication, between the optoelectronic module and a host, of diagnostic parameter information concerning the optoelectronic component; and

a pinout arrangement comprising:

a pin array having a set of pins configured ("20-pin SCA-2 Connector to Host" in Figure 1) and arranged for substantial conformity with the SFF configuration standard (pages 3-7, "3 Introduction and overview"); and

a pair of pins in communication with the serial digital interface (serial clock signal "SCL" on pin 5 and serial data signal "SDA" on pin 6), each of the pair of pins also being configured and arranged for communication with the host by way of a corresponding interface line (pages 12-13, Table 8 and "5.2.1 Serial module definition protocol" and pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)").

Regarding **claims 2 and 39**, SFF Committee discloses that the optoelectronic component comprises a transmit optical subassembly; and a receiver optical subassembly (including "Optical Receiver" and "Laser" as shown in Figure 1).

Regarding **claims 4, 19, and 41**, SFF Committee discloses that the controller IC is configured to receive from the host, by way of at least one of the pair of pins, data (pages 12-13,

Table 8 and "5.2.1 Serial module definition protocol" and pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)").

Regarding **claims 5, 20, and 42**, SFF Committee discloses that one of the pair of pins is configured to communicate with the host by way of an SDA interface line, and the other of the pair of pins is configured to communicate with the host by way of an SCL interface line (pages 12-13, Table 8 and "5.2.1 Serial module definition protocol").

Regarding **claims 6 and 21**, SFF Committee discloses that the pin array is configured and arranged for substantial conformity with the SFF configuration standard (pages 3-7, "3 Introduction and overview").

Regarding **claims 8, 23, and 44**, SFF Committee discloses that the diagnostic parameter information includes alarm information (such as TX_FAULT; pages 3-7, "3 Introduction and overview").

Regarding **claims 9, 24, and 45**, SFF Committee discloses that one of the pair of pins comprises a serial communication data pin ("SDA") and the other of the pair of pins comprises a serial communication clock pin ("SCL"; pages 12-13, Table 8 and "5.2.1 Serial module definition protocol").

Regarding **claims 10 and 25**, SFF Committee discloses that the pair of pins is configured for repeated pluggability (pages 20-29, "6 Mechanical interface for all GBICs").

Regarding **claim 11**, SFF Committee discloses that the controller IC is configured to generate at least one of a temperature dependent output and a temperature independent output, at least in the sense that SFF Committee discloses that the controller IC is configured to generate

outputs, and any such outputs are inherently either "temperature dependent" or "temperature independent."

Regarding **claim 13**, SFF Committee discloses that the serial digital interface substantially conforms to one of a GBIC standard; and, the SFF standard (pages 3-7, "3 Introduction and overview"; and pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)").

Regarding **claims 14 and 32**, SFF Committee discloses that the optoelectronic module is configured to receive a "rate select" signal from the host by way of one of the pins of the pinout arrangement (pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)," particularly page 50, Table D.7).

Regarding **claims 15, 35**, SFF Committee discloses that the optoelectronic module is configured to transmit a "transmitter fault" signal to the host by way of one of the pins of the pinout arrangement (pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)," particularly page 50, Table D.7).

Regarding **claims 16 and 46**, SFF Committee discloses a plurality of memory mapped locations, at least one of which is accessible by way of the serial digital interface and which is configured to receive and store information concerning at leas one diagnostic parameter (in an E^2PROM; pages 12-13, "5.2.1 Serial module definition protocol"; and pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)").

Regarding **claim 27**, SFF Committee discloses that at least one of the plurality of memory mapped locations is configured to be read, and written to, by way of the serial digital interface (pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)").

Regarding **claim 29**, SFF Committee discloses that the diagnostic parameter information stored in the at lest one memory mapped location is in a digitized form (pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)").

Regarding **claim 31**, SFF Committee discloses a laser driver, a post-amplifier, and a power controller (page 4, Figure 1).

Regarding **claim 33**, SFF Committee discloses that the "rate select" signal includes at least "high" and "low" values, each of which corresponds to a different data rate (pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)").

Regarding **claim 34**, SFF Committee discloses that the "rate select" signal is received from the host by way of one of the pair of pins (pages 12-13, "5.2.1 Serial module definition protocol"; pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)," particularly page 50, Table D.7).

Regarding **claim 36**, SFF Committee discloses that the "transmitter fault" signal is transmitted to the host by way of one of the pair of pins (pages 12-13, "5.2.1 Serial module definition protocol"; pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)").

Regarding **claim 37**, SFF Committee disclose a memory map table associated with at least one of the plurality of memory map locations comprises information indicating at least a storage location of a configuration value for a diagnostic parameter (pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)," particularly page 44, Table D.1).

Regarding **claims 47 and 50**, SFF Committee disclose that the pin array includes the pair of pins such that the pair of pins is used for multiple and different types of signals, at least one of

which is digital parameter information (pages 12-13, "5.2.1 Serial module definition protocol"; and pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)").

Regarding **claims 49 and 52**, SFF Committee et al. disclose memory (e.g., E^2PROM); and a memory interface for allowing a host device to read from and write to memory mapped locations within the memory in accordance with commands received from a host device, wherein the memory interface allows the host device to read digital values corresponding to the diagnostic parameter information from the memory mapped locations through the pair of pins (i.e., through the serial interface; pages 12-13, "5.2.1 Serial module definition protocol"; and pages 44-52, "Annex D: Module definition "4" GBIC (Serial Identification)").

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 3, 18, 26, and 40** are rejected under 35 U.S.C. 103(a) as being unpatentable over **SFF Committee** in view of **Keevill et al.** (US 6,359,938 B1).

Regarding **claims 3, 18, and 40**, SFF Committee discloses a system as discussed above with regard to claims 1, 17, and 38, including a serial digital interface but does not specifically disclose I2C or MDIO serial communication. However, various serial interface standards are well known in the communications art. Keevill et al. in particular teach a system that is related to the one described by SFF Committee including a communications device 146 that communicates with a host device via a serial interface 142 (Figure 12). Keevill et al. further teach that the serial

interface is compatible with I2C serial communication (Figure 55; column 37, lines 1-8). Regarding claims 3, 18, and 40, it would have been obvious to a person of ordinary skill in the art to use a I2C serial communication standard as taught by Keevill et al. in the system disclosed by SFF Committee as an engineering design choice of a serial communication standard in order to allow the system to properly communicate with a particular host device as already disclosed by SFF Committee.

Regarding **claim 26,** SFF Committee discloses a system as discussed above with regard to claims 17, including a plurality of memory mapped locations but does not specifically disclose registers. However, various types of memory elements, including registers, are well known in the electronic and communication arts, and Keevill et al. in particular teach using registers to store data values (column 7, lines 43-46). It would have been obvious to a person of ordinary skill in the art to specifically provide a register as taught by Keevill et al. in the system disclosed by SFF Committee as an engineering design choice of a way to effective implement the storage element already disclosed and thereby store values for later retrieval.

7. **Claims 7, 22, 30, and 43** are rejected under 35 U.S.C. 103(a) as being unpatentable over **SFF Committee** in view of **Baltz et al.** (US 6,469,906 B1).

Regarding **claims 7, 22, 30, and 43**, SFF Committee discloses a system as discussed above with regard to claim 1, 17, and 38, including a pin array conforming to a SFF standard. Regarding claims 7, 22, and 43 in particular, SFF Committee does not explicitly disclose that the pin array comprises one of a 2x5 pin arrangement; and, a 2x10 pin arrangement. Regarding claim 30 in particular, SFF Committee does not explicitly disclose that the pin array comprises two rows of six pins each. However, SFF Committee already disclose that the pin array comprises

pins, wherein each pin comprises one of the following: a serial communication data pin; a receiver ground pin; a receiver power pin, a signal detect pin; a receive data inverted pin; a receive data pin; a serial communication clock pin; a transmitter power pin; a transmitter ground pin; a transmitter disable pin; a transmit data pin; a transmit data inverted pin; an interrupt pin; and a loss of signal pin (pages 3-7, "3 Introduction and overview").

Further regarding claims 7, 22, 30, and 43, it is well understood in the art that a physical arrangement of pins in a module may be designed to conform to an industry standard such as already suggested by SFF Committee in order to ensure that the module is compatible with other devices. Baltz et al. further suggest an optical transceiver module that is related to the ones disclosed by SFF Committee, and that may conform to a SFF standard and have pin array comprising a 2x5 or a 2x6 pin arrangement (based on conforming to that standard; column 1, lines 52-65). Regarding claims 7, 22, 30, and 43, it would have been obvious to a person of ordinary skill in the art to ensure that the pins have a 2x5 or 2x6 pin array arrangement as taught by Baltz et al in the system disclosed by SFF Committee in order to ensure that the module has a standard physical arrangement that is compatible with other components in a larger system.

8. **Claims 12 and 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over **SFF Committee** in view of **Levinson** (US 5,019,769 A).

Regarding **claim 12**, SFF Committee discloses a system as discussed above with regard to claim 1 including a controller IC but does not explicitly disclose an analog monitoring connection. However, Levinson teaches a system that is related to the one disclosed by SFF Committee, including an optical transmitter (laser diode 100) with a controller IC (microcontroller 162) and connected to a host via a serial interface 200 (Figures 3 and 12). King

et al. further teach that the controller IC further comprises an analog monitoring connection (column 4, lines 19-68; column 5, lines 1-18). It would have been obvious to a person of ordinary skill in the art to include an analog monitoring connection as taught by Levinson in the system disclosed by SFF Committee in order to advantageously enable the controller to monitor characteristics such as temperature from a sensor and provide appropriate control signals in response.

Regarding **claim 28**, SFF Committee discloses a system as discussed above with regard to claim 17 including memory mapped locations but does not explicitly disclose that at least one of the memory mapped locations is configured to receive and store information concerning at least one bias current associated with the transmit optical subassembly; optical transmit power associated with the transmit optical subassembly; received signal power; supply voltage; laser temperature; operation time; and, polarity and type of input and output signals.

However, Levinson further teaches using memory locations (e.g., in EEPROM 166) configured to receive and store information including optical transmit power and laser temperature (column 4, lines 20-32; column 6, lines 40-45; column 9, lines 1-35; column 10, lines 57-66). It would have been obvious to a person of ordinary skill in the art to store values including optical transmit power and laser temperature as taught by Levinson in the system disclosed by SFF Committee in order to advantageously monitor changes in those qualities over time and predict potential failure of the optoelectronic device prior to the failure (Levinson, column 9, lines 1-14).

9. **Claims 48 and 51** are rejected under 35 U.S.C. 103(a) as being unpatentable over **SFF Committee**.

Regarding **claims 48 and 51**, SFF Committee discloses a system as discussed above with regard to claim 1 and 38, including a pin array conforming to a SFF standard but does not explicitly disclose that the pin array has a plurality of pins arranged in two rows, and the pair of pins is not aligned with either of the two rows. However, it is well understood in the art that electronic and optoelectronic modules may have various physical arrangements of pins. Regarding claims 48 and 51, it would have been obvious to a person of ordinary skill in the art to provide a plurality of pins arranged in two rows and the pair of pins not aligned with either of the two rows, as an engineering design choice of a way to physically arrange the pins in the module disclosed by SFF Committee. The claimed differences exist not as a result of an attempt by Applicants to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art.

Response to Arguments

10. Applicant's arguments filed 09 April 2007 with respect to claims 1-52 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christina Y. Leung whose telephone number is 571-272-3023. The examiner can normally be reached on Monday to Friday, 7:30 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christina Y Leung

CHRISTINA LEUNG
PRIMARY EXAMINER